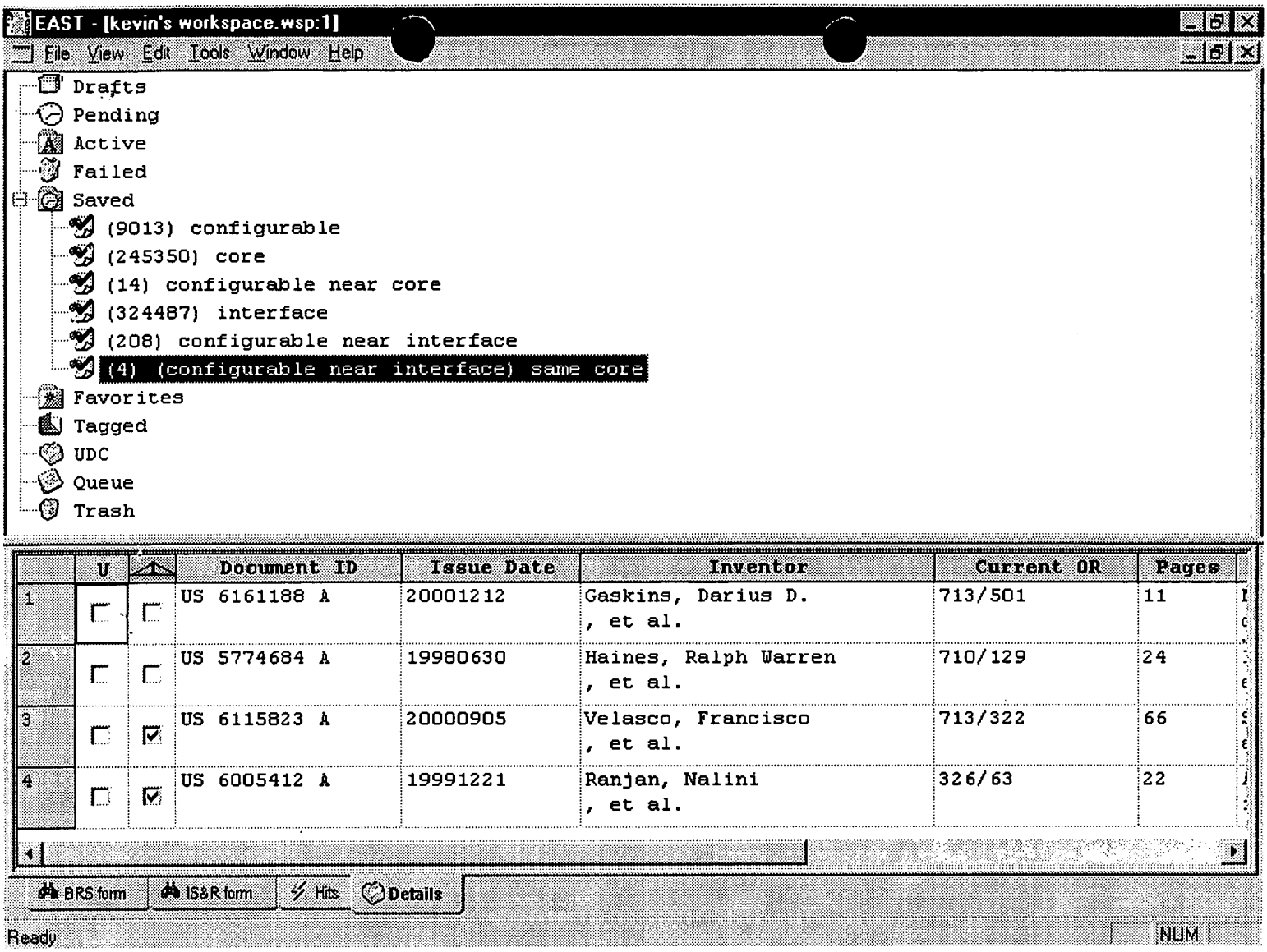
	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
12	BRS	2	coreconnect	IBM_TDB	2003/07/25 10:13		
13	BRS	419	routing same reconfigurable	USPAT; US-PGPUB; DERWENT; IBM_TDB	2003/07/25 10:13		
14	BRS	293	routing same reconfigurable and components	USPAT; US-PGPUB; DERWENT; IBM_TDB	2003/07/25 10:13		
15	BRS	29	routing same reconfigurable and components and hdl	USPAT; US-PGPUB; DERWENT; IBM_TDB	2003/07/25 10:18		
16	BRS	26	routing same reconfigurable and components and hdl and interconnect	USPAT; US-PGPUB; DERWENT; IBM_TDB	2003/07/25 10:18		
17	BRS	24	routing same reconfigurable and components and hdl and interconnect and user	USPAT; US-PGPUB; DERWENT; IBM_TDB	2003/07/25 10:23		
18	BRS	18	routing same reconfigurable and components and hdl and interconnect and user and (latency or bandwidth)	USPAT; US-PGPUB; DERWENT; IBM_TDB	2003/07/25 13:55		
21	BRS	13	routing same reconfigurable and components and hdl and interconnect and (display or terminal or IO) and (latency or bandwidth)	USPAT; US-PGPUB; DERWENT; IBM_TDB	2003/07/25 14:40		
22	BRS	447	reconfigurable same computing	USPAT; US-PGPUB; DERWENT; IBM_TDB	2003/07/25 15:14		
29	BRS	1773	interface same configurable and signal and parameters	USPAT; US-PGPUB; DERWENT	2003/07/27 16:23		
30	BRS	3	interface same configurable same parameters and compilation and integrated adj circuit and display	USPAT; US-PGPUB; DERWENT	2003/07/27 16:54		
31	BRS	37	interface same configurable same parameters and integrated adj circuit and display	USPAT; US-PGPUB; DERWENT	2003/07/27 16:55		

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
32	BRS	62	interface same configurable same parameters and integrated adj circuit	USPAT; US-PGPUB; DERWENT	2003/07/27 16:56		
33	BRS	71	(interface same configurable and signal and parameters) and (hdl or vhdl)	USPAT; US-PGPUB; DERWENT	2003/07/27 17:06		
34	BRS	44	((interface same configurable and signal and parameters) and (hdl or vhdl)) and (compile or compilation)	USPAT; US-PGPUB; DERWENT	2003/07/28 07:42		


EAST - [kevin's workspace.wsp:1]
File View Edit Tools Window Help
Drafts
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(9013) configurable
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(324487) interface
(208) configurable near interface
(4) (configurable near interface) same core
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1
US 6161188 A
20001212
Gaskins, Darius D. , et al.
713/501
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2
US 5774684 A
19980630
Haines, Ralph Warren , et al.
710/129
24
3
US 6115823 A
20000905
Velasco, Francisco , et al.
713/322
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US 6005412 A
19991221
Ranjan, Nalini , et al.
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BRS form
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In general, synchronous circuits, such as edge triggered D flip flops, can be used to reliably capture and transmit signals on either the positive-edge or the negative-edge of a clock pulse or strobe. A noise burst on a signal line between clock pulses does not typically upset a synchronous circuit. While synchronous circuits have been included in I/O interfaces for testing purposes (e.g., scan testing), they are not typically used to capture data signals communicated between core logic and pads in an integrated circuit chip. To reliably capture such data signals, synchronous circuits must have clocks that abide by a variety of constraints including skew, duty cycle, and setup/hold times. If these clock parameters are violated, the synchronous circuits could malfunction (e.g., clock race, latch-up) resulting in erroneous data signals being captured and transmitted. To reduce the probability of synchronous circuits malfunctioning, such circuits can be designed using custom physical layouts.

Custom physical layouts place physical placement control and constraints on the components of the I/O interface so as to restrict the variability of critical parameters, thereby ensuring reliable high frequency operation. By designing components to have a tight relationship to each other, any uncertainty in the operation and/or compensation of such components can be minimized. For example, clock and data paths can be accurately matched as well as designed to compensate for simultaneous switching push-out.

In addition to reliability concerns, it is also desirable that I/O interfaces be configurable on-the-fly to comply with multiple protocols and signal specifications including: Accelerated Graphics Port (AGP), Double Data Rate (DDR), Peripheral Component Interconnect (PCI), Stob Serial Terminated Logic (SSTL), and Transistor-to-Transistor Logic (TTL). Such I/O interfaces provide additional flexibility to system designers.

Accordingly, there is a need for reliable and flexible I/O interfaces for buffering and conditioning data signals between core logic and pads in integrated circuit chips. It is desirable that these I/O interfaces be configurable on-the-fly to comply with multiple protocols and signal specifications. Such I/O interfaces should have custom physical layouts of circuitry, power, and clock bussing to eliminate problems associated with, for example, uneven layout traces.

SUMMARY OF THE INVENTION

The present invention is directed to reliable I/O interfaces for an integrated circuit chip that can be configured on-the-fly to comply with a

multiplexer 375 is communicated to MBA clock tree 250 (see FIG. 21) which generates amplified/buffered non-inverted (mba.sub.-- clk) 380 and inverted (mbaclk.sub.-- n) 381 versions of the signal onto the MBA bus 202. A bus cycle (cycle) signal 382 is received by MBA arbiter 248 from a master module after it received a grant to access the bus and operates to inform every other module that a bus access cycle has started.

Those workers having ordinary skill in the art in light of the description provided herein, will appreciate that the inventive dynamic task power management structure and method provide additional power savings to the distributed power management method of the MBA Architecture, without significant impact on the overall system performance.

Aspects of this embodiment of the invention are expected to provided further benefits when faster memory devices become available, for example, dual-data rate synchronous data RAM, Also, for RAMBUS memory, it will be possible to shift data at both edges of a clock.

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FAST MBA WITH CONFIGURABLE INTERFACE AND SINGLE-EDGE OR DUAL-EDGE FIFO

We now describe alternative embodiments for a modular bus architecture (MBA) and fast modular bus architecture (FMBA) having a configurable interface and either single-edge FIFO or double-edge FIFO.

Dual-Edge FIFO Interface

We now describe one dual-edge embodiment of the FIFO interface with respect to FIG. 31. Dual-Edge FIFO (DFIFO) 401 provides means to interconnect internal modules at FMBA/MBA back-end level (core logic level) 402, block level (MBA/FMBA module level) 403, or chip level (usually including the processor and one or more MBA modules) 404 for reused purposes. DFIFO typically includes three primary modules or components: (i) host FIFO interface 405, (ii) target FIFO interface 406, and (iii) RAM (or register block) 407. The FIFO or DFIFO is used as a back end interface because it is very easy to design to, as many workers having ordinary skill in the art are familiar with interfacing generic FIFOs. The host interface 405 is responsible for accepting data from host side 408 and flags situations it is full or when valid read data is present in the read data FIFO. Target Interface 406 on the target side 413 is responsible for transferring data out from FIFO 410, accepting read data from target core module 411, and flags when the read data FIFO is full.

activity and is responsible for self-controlling its operating condition to minimize power consumption. Each device includes a first component which operates continuously so as to provide the monitoring functionality and a second component that operates in a low power consumption mode unless first component signals the second component that its operation is needed during that time period. The first component withholds a device operating input from the second component when none of the communicated identifiers match the particular device; and provide the device operating input to the second component when one of said communicated device identifiers match that particular device. The number of circuit components is reduced to a minimum in the first component so that the number of circuit elements which are continuously active are reduced. In one embodiment of the invention, the device operating input is a clock signal operating at the bus clock frequency. Power consumption is reduced due to the reduction in the number of circuits which are actively clocked. The inventive structure and method provide very fine temporal control of power consumption in the computer system.

In another aspect, the invention provides structure and method for a modular bus architectural (MBA) and fast modular bus architectural (FMBA) frames for System-on-a-Chip (SOC) designs including MBA/FMBA library modules that decrease design time. In another aspect, the invention provides structure and method for adjusting bus clock speed in accordance with bus activity and task performance requirements so that further control of power consumption in the system is achieved without sacrificing performance. In one embodiment, the clock rate is adjusted in accordance with preassigned performance factors associated either with a functional unit or with a task type so that the task completes within a desired time without unnecessary power consumption. In another aspect, the FMBA/MBA is provided with a configurable interface that provides alternative single-edge and double-edge First-In-First-Out buffers. Among other advantages, these FIFO structures permit interconnection of MBA/FMBA modules at the core logic level, MBA/FMBA block level, and chip level so that systems are readily and reliable designed and implemented with minimum redesign.

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DRAWING DESCRIPTION:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagrammatic representation of portions of a conventional centralized power management system.

FIG. 2 is a diagrammatic representation of a first embodiment of a computer

gated clock signal (gw.sub.-- clk) 558.

The data output of the FIFOs is read out with the read clock signal (r.sub.-- clk) 573 and the control signals read address (ra) 571 and read enable (r.sub.-- en) 572 supplied by the FIFO control state machine. The data output from write data RAM 551, referred to as data out 1 (data.sub.-- o.sub.-- 1) 581, corresponds to positive edge data only. The data output coming from the second write data RAM 552, referred to as data out 2 (data.sub.-- o.sub.-- 2) 582, is positive edge or negative edge sample data depending on the write operation selected via multiplexers 564, 565 as described above. The output multiplexer 577 is control by the state machine depending on the dual edge or single edge configuration mode register bit dual edge select signal 566.

FIG. 39 illustrates an exemplary embodiment of a Read Data FIFO RAM (or Register Block) structure 584 to handle data in/out on dual-edge clock or single-edge clock only. This is a different physical buffer for read operations and effectively operates in the reverse direction relative to the write buffer in FIG. 38. It is readily apparent from the structure and the signals, that the structure and operation is very much similar to that just described for the write data FIFO RAM 550 in FIG. 38, except that the read data RAM generates a read FIFO data (f.sub.-- rf.sub.-- dato) signal 585 at its output 586, in response to an enable data out signal (e.sub.-- out) 590.

The inventive dual-edge FIFO features provide and/or support: (i) Parameterized synchronous or asynchronous FIFO, (ii) Parameterized RAM size and RAM data bus width, (iii) Parameterized data rate transfer (either singular (positive) edge clocking or dual-edge clocking), (iv) configurable to support different combinational Write Parameter RAM and Write Data RAM, or Write Parameter RAM and Read Data RAM, or write data RAM only without read; (v) Flushing of current FIFO request, and flushing of entire FIFO requests may be used in case error occurs; and (vi) Parameterized control bit register "enough space acknowledge" (req.sub.-- esp.sub.-- ack) to indicate FIFO go-ahead to request target access even if not all write data is in the memory yet.

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Host Write Cycle And Parameter.

We now describe operation during a host write cycle relative to the diagram in FIG. 42. The host initiates a write cycle request by asserting a request to access FIFO signal (rq.sub.-- f) and keeping it until FIFO

asserts FIFO acknowledges request from host (f.sub.-- ack). Host makes